CLAIMS

1. A transistor formed on a semiconductor substrate of a first conductivity type and comprising:

a well formed in said substrate and doped with said first conductivity type to an impurity level higher than that of said substrate;

a drain region doped to a second conductivity type opposite to said first conductivity type disposed in said well;

a pair of opposed source regions doped to said second conductivity type disposed in said well and separated from opposing outer edges of said drain region by channel regions, said pair of opposed source regions electrically coupled together;

a pair of gates disposed above and insulated from said channel regions, said gates electrically coupled together; and

a region of said well disposed below said drain region doped so as to reduce capacitive coupling between said drain region and said well.

2. A transistor formed on a p-type semiconductor substrate and comprising:

a p-well formed in said substrate and doped to an impurity level higher than that of said substrate;

an n-type drain region disposed in said p-well;

a pair of opposed n-type source regions disposed in said p-well and separated from opposing outer edges of said drain region by channel regions, said pair of opposed n-type source regions electrically coupled together;

a pair of gates disposed above and insulated from said channel regions, said gates electrically coupled together; and

a region of said p-well disposed below said drain region doped so as to reduce capacitive coupling between said drain region and said p-well.

3. A transistor disposed on a p-type substrate comprising:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate-doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate.

4. The transistor of claim 3 wherein said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels.

5. A transistor disposed on a p-type substrate comprising:

an n-well disposed in said p-type substrate, a portion of said n-well more lightly doped than the remainder of said n-well;

a P+ drain region disposed in said lightly-doped region of said n-well, a periphery of said P+ drain region extending beyond an outer boundary of said lightly-doped region of said n-well, said periphery surrounded by a lightly-doped P region;

a pair of P+ source regions spaced apart from opposite edges of said P+ drain region at a distance sufficient to form first and second channels, each of said P+ source regions surrounded by a lightly doped P region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate.

6. The transistor of claim 5 wherein said periphery of said P+ drain region extends laterally into said p-well beyond said outer boundary of said lightly-doped region of said n-well a distance about equal to that of said first and second channels.

7. In an integrated circuit formed on a p-type substrate, an output driver circuit coupled between an internal circuit on the integrated circuit and an input/output pad on the integrated circuit comprising;

a first transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate

doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

a second transistor including:

an n-well disposed in said p-type substrate, a portion of said n-well more lightly doped than the remainder of said n-well;

a P+ drain region disposed in said lightly-doped region of said n-well, a periphery of said P+ drain region extending beyond an outer boundary of said lightly-doped region of said n-well, said periphery surrounded by a lightly-doped P region;

a pair of P+ source regions spaced apart from opposite edges of said P+ drain region at a distance sufficient to form first and second channels, each of said P+ source regions surrounded by a lightly doped P region and electrically coupled together;

a first gate region disposed above and insulated from said first channel; and

a second gate region disposed above and insulated from said second channels and electrically coupled to said first gate;

wherein said drain of said first transistor and said drain of said second transistor are coupled to said input output pad, said source regions of said first transistor are coupled to ground, said source regions of said second transistor are coupled to a supply potential, and said gate regions of said first transistor and said second transistor are coupled to an output of said internal circuit.

8. The output driver circuit of claim 7 wherein:

in said first transistor said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels of said first transistor; and

in said second transistor said periphery of said P+ drain region extends laterally into said p-well beyond said outer boundary of said lightly-doped region of said n-well a distance about equal to that of said first and second channels of said second transistor.

9. An output driver circuit for an integrated circuit formed on a p-type substrate comprising;

a buffer coupled between an internal circuit in said integrated circuit and an input/output pad of said integrated circuit; and

a transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

said drain region of said transistor coupled to said input output pad, said source regions of said transistor coupled to ground and said gate regions of said transistor coupled together to ground through an impedance-matching resistor.

10. The output driver circuit of claim 9 wherein in said transistor said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels.

11. An input driver circuit for an integrated circuit formed on a p-type substrate comprising;

a buffer coupled between an input/output pad of said integrated circuit and internal circuit in said integrated circuit; and

a transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending

laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

said drain region of said transistor coupled to said input output pad, said source regions of said transistor coupled to ground and said gate regions of said transistor coupled together to ground through an impedance-matching resistor.

12. The input driver circuit of claim 11 wherein in said transistor said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels.

13. A differential output driver circuit for an integrated circuit formed on a p-type substrate comprising;

a differential buffer having an input coupled to an output of an internal circuit in said integrated circuit, a non-inverting output coupled to a first input/output pad of said integrated circuit and an inverting output coupled to a second input/output pad of said integrated circuit; and

a first transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer edge of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

said drain region of said first transistor coupled to said first input output pad, said source regions of said first transistor coupled to ground and said gate regions of said first transistor coupled together to ground through an impedance-matching resistor;

a second transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first

and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

said drain region of said second transistor coupled to said second input output pad, said source regions of said second transistor coupled to ground and said gate regions of said second transistor coupled together to ground through an impedance-matching resistor.

14. The differential output driver circuit of claim 13 wherein:

in said first transistor said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels of said first transistor; and

in said second transistor said periphery of said P+ drain region extends laterally into said p-well beyond said outer boundary of said lightly-doped region of said n-well a distance about equal to that of said first and second channels of said second transistor.

15. A differential input driver circuit for an integrated circuit formed on a p-type substrate comprising;

a differential buffer having a non-inverting input coupled to a first input/output pad of said integrated circuit, an inverting input coupled to a second input/output pad of said integrated circuit, said differential buffer having an output coupled to an internal circuit in said integrated circuit; and

a first transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

said drain region of said first transistor coupled to said first input output pad, said source regions of said first transistor coupled to ground and said gate regions of said first transistor coupled together to ground through an impedance-matching resistor;

a second transistor including:

a p-well disposed in the p-type substrate, said p-well doped to a higher concentration than said substrate and having a substrate-doped portion therein doped to about the same concentration as said substrate, said substrate-doped portion extending vertically from an upper surface of said p-well to said substrate;

an N+ drain region disposed in said substrate-doped portion of said P-well, a periphery of said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well, said periphery surrounded by a lightly doped N region;

a pair of N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first

and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together;

a first gate disposed above and insulated from said first channel; and

a second gate disposed above and insulated from said second channels and electrically coupled to said first gate;

said drain region of said second transistor coupled to said second input output pad, said source regions of said second transistor coupled to ground and said gate regions of said second transistor coupled together to ground through an impedance-matching resistor.

16. The differential input driver circuit of claim 15 wherein:

in said first transistor said periphery of said N+ drain region extends laterally into said p-well beyond said outer boundary of said substrate-doped portion of said p-well a distance about equal to that of said first and second channels of said first transistor; and

in said second transistor said periphery of said P+ drain region extends laterally into said p-well beyond said outer boundary of said lightly-doped region of said n-well a distance about equal to that of said first and second channels of said second transistor.

17. A method for forming a transistor comprising:

forming an implant mask over a region on a p-type semiconductor substrate;

forming a p-well in said substrate, said masked region preventing implantation of p-well dopant in a portion of said substrate to leave a substrate-doped region within said p-well extending to a bottom of said p-well;

removing said mask;

forming an N+ drain region at said substrate-doped region in said substrate, said N+ drain region extending laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well;

forming opposed N+ source regions spaced apart from opposite edges of said N+ drain region at a distance sufficient to form first and second channels, each of said N+ source regions surrounded by a lightly doped N region and electrically coupled together; and

forming a first gate disposed above and insulated from said first channel and a second gate disposed above and insulated from said second channels and electrically coupled to said first gate.

18. The method of claim 17 wherein forming said N+ drain region includes forming said N+ drain region to extend laterally into said p-well beyond an outer boundary of said substrate doped portion of said p-well a distance about equal to that of said first and second channels of said first transistor.

19. A method for forming a transistor comprising:

forming an n-well in said p-type substrate, a portion of said n-well more lightly doped than the remainder of said n-well;

forming a P+ drain region disposed in said lightly-doped region of said n-well, a periphery of said P+ drain region extending beyond an outer boundary of said lightly-doped region of said n-well, said periphery surrounded by a lightly-doped P region;

forming a pair of P+ source regions spaced apart from opposite edges of said P+ drain region at a distance sufficient to form first and second channels, each of said P+ source regions surrounded by a lightly doped P region and electrically coupled together; and

forming a first gate disposed above and insulated from said first channel and a second gate disposed above and insulated from said second channels and electrically coupled to said first gate.

20. The method of claim 19 wherein forming said P+ drain region includes forming said P+ drain to extend laterally into said p-well beyond said outer boundary of said lightly-doped region of said n-well a distance about equal to that of said first and second channels of said second transistor.

21. The method of claim 19 wherein forming an n-well in said p-type substrate, a portion of said n-well more lightly doped than the remainder of said n-

well comprises forming said n-well and counterdoping said n-well to form said portion of said n-well more lightly doped than the remainder of said n-well.